

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

**Applicant(s):** Fook-Luen Heng, et al.

**Docket:** END920030090US1 (16992)

**Serial No.:** Unassigned

**Dated:**

**Filed:** Herewith

**For:** LAYOUT OPTIMIZATION UNDER  
CONSTRAINTS ON EDGE PLACEMENT

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**INFORMATION DISCLOSURE STATEMENT**

Sir:

In accordance with 37 C.F.R. §§ 1.97 and 1.98, it is requested that the following references, which are also listed on the attached Form PTO-1449, be made of record in the above-identified case.

1. U.S. Patent No. 4,805,113, dated February 14, 1999 to Ishii, et al.;
2. U.S. Patent No. 5,416,722, dated May 16, 1995 to Edwards;
3. U.S. Patent No. 5,515,293, dated May 7, 1996 to Edwards;
4. U.S. Patent No. 5,568,396, dated October 22, 1996 to Bamji, et al.;

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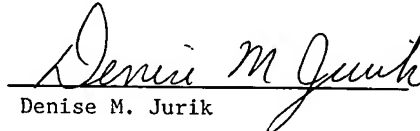
**CERTIFICATE OF MAILING BY "EXPRESS MAIL"**

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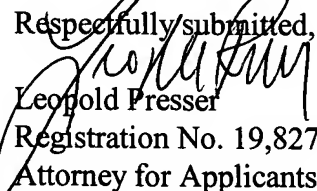
I hereby certify that this correspondence is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. §1.10 on the date indicated above and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Dated: 02/10/04

  
Denise M. Jurik

5. U.S. Patent No. 5,581,474, dated December 3, 1996 to Bamji, et al.;
6. U.S. Patent No. 5,612,893, dated March 18, 1997 to Hao, et al.;
7. U.S. Patent No. 5,764,532, dated June 9, 1998 to Patel;
8. U.S. Patent No. 5,825,661, dated October 20, 1998 to Drumm;
9. U.S. Patent No. 5,889,681, dated March 30, 1999 to Suda;
10. U.S. Patent No. 5,892,261, dated April 6, 1999 to Lin, et al.;
11. U.S. Patent No. 6,434,721 B1, dated August 13, 2002 to Chiluvuri, et al.;
12. PCT International Publication No. WO 01/65424 A2, dated September 7, 2001;
13. J. L. Burns, et al., "Detection of Overconstraints in IC Layout Compaction", IBM Technical Disclosure Bulletin, Vol. 35, No. 4B, September 1992, Pages 466-469;
14. J. Lee, "Systematic Formulation of Design Rules for Integrated Circuit Layouts", IBM Technical Disclosure Bulletin, Vol. 30, No. 7, December 1987, Pages 120-123; and
15. David Marple, "A Hierarchy Preserving Hierarchical Compactor" in Proceedings of the 27th ACM/IEEE Design Automation Conference (1990), Page 375.

Applicants are submitting a copy of the above-cited non-U.S. patents. Inasmuch as this Information Disclosure Statement is being submitted in accordance with the schedule set out in 37 C.F.R. § 1.97(b), no statement or fee is required.

Respectfully submitted,  
  
Leopold Presser  
Registration No. 19,827  
Attorney for Applicants

SCULLY, SCOTT, MURPHY & PRESSER  
400 Garden City Plaza  
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(516) 742-4343

LP:jy

**LIST OF REFERENCES  
CITED BY APPLICANT**

(Use several sheets if necessary)

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**U.S. PATENT DOCUMENTS**

EXAMINER INITIAL*		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (if appropriate)
	AA	4,805,113	2/14/99	Ishii, et al.			
	AB	5,416,722	5/16/95	Edwards			
	AC	5,515,293	5/7/96	Edwards			
	AD	5,568,396	10/22/96	Bamji, et al.			
	AE	5,581,474	12/3/96	Bamji, et al.			

		Foreign Document Number	Date	Country	CLASS	SUBCLASS	TRANSLATION	
							YES	NO
		WO 01/65424 A2	9/7/01	PCT				

**OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, Etc.)**

	J. L. Burns, et al., "Detection of Overconstraints in IC Layout Compaction", IBM Technical Disclosure Bulletin, Vol. 35, No. 4B, September 1992, Pages 466-469;
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\* **EXAMINER:** Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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	AF	5,612,893	3/18/97	Hao, et al.			
	AG	5,764,532	6/9/98	Patel			
	AH	5,825,661	10/20/98	Drumm			
	AI	5,889,681	3/30/99	Suda			
	AJ	5,892,261	4/6/99	Lin, et al.			

		Foreign Document Number	Date	Country	CLASS	SUBCLASS	TRANSLATION	
							YES	NO

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	AK	6,434,721 B1	8/13/02	Chiluvuri, et a.			
	AL						
	AM						
	AN						
	AO						

		Foreign Document Number	Date	Country	CLASS	SUBCLASS	TRANSLATION	
							YES	NO

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